

**What is claimed is:**

1           1.    A damascene gate process, comprising:  
2           providing a semiconductor substrate having a pad layer  
3                 and a etch stop layer formed thereon;  
4           forming an insulating layer to cover the etch stop layer;  
5           forming an opening be partially removing the insulating  
6                 layer, the etch stop layer, and the pad layer;  
7           forming a protective spacer on the sidewall of the opening,  
8                 wherein the tops of the protective spacer are lower  
9                 than the insulating layer;  
10          forming a gate conducting layer in the opening;  
11          removing the protective spacer and the insulating layer  
12                 to expose a portion of the semiconductor substrate  
13                 and the etch stop layer;  
14          implanting the exposed semiconductor substrate to form  
15                 lightly doped drains;  
16          forming a gate spacer to cover the gate conducting layer;  
17          removing the etch stop layer and the pad layer to expose  
18                 portions of the semiconductor substrate; and  
19          implanting the exposed semiconductor substrate to form  
20                 source/drain.

1           2.    The damascene gate process of claim 1, wherein the  
2           pad layer is an oxide layer.

1           3.    The damascene gate process of claim 1, wherein the  
2           etch stop layer is a nitride layer.

1           4.    The damascene gate process of claim 1, wherein the  
2           insulating layer is a tetraethylorthosilane layer.

1           5.     The damascene gate process of claim 1, wherein the  
2     protective spacer are nitride layers.

1           6.     The damascene gate process of claim 1, wherein the  
2     gate conducting layer is a laminated construction with two  
3     conducting layers.

1           7.     The damascene gate process of claim 6, wherein the  
2     conducting layer is a poly layer, a SiW layer, a W layer, or  
3     a silicide layer.

1           8.     The damascene gate process of claim 1, wherein the  
2     gate spacer is a nitride layer.

1           9.     The damascene gate process of claim 1, before the  
2     step of forming the gate conducting layer, further comprising  
3     a step of forming a gate oxide layer on the exposed semiconductor  
4     substrate of the bottom opening.

1           10.    The damascene gate process of claim 1, wherein the  
2     insulating layer is removed by HF or BHF.

1           11.    A damascene gate process, comprising:  
2     providing a semiconductor substrate having a plurality  
3                of shallow trench isolation (STI) structures, an  
4                STI protective layer is formed on each of the STI  
5                structures;  
6     sequentially forming a pad layer and an etch stop layer  
7                between the STI structures;  
8     forming an insulating layer to cover the STI structures  
9                and the etch stop layer;

10 forming an opening between the structures by partially  
11 removing the insulating layer, the etch stop layer,  
12 and the pad layer;  
13 forming a protective spacer on the sidewall of the opening,  
14 wherein the tops of the protective spacer are lower  
15 than the insulating layer;  
16 forming dissimilar conducting layers acting as gate  
17 conducting layer in the bottom of the opening;  
18 removing the protective spacer and the insulating layer  
19 to expose a portion of the semiconductor substrate  
20 and the etch stop layer;  
21 implanting the exposed semiconductor substrate to form  
22 lightly doped drains beside the gate conducting  
23 layer;  
24 forming a gate spacer to cover the gate conducting layer;  
25 removing the etch stop layer and the pad layer; and  
26 implanting the exposed semiconductor substrate to form  
27 source/drain.

1 12. The damascene gate process of claim 11, wherein the  
2 STI structures are oxide layers.

1 13. The damascene gate process of claim 11, wherein the  
2 STI protective layer is a nitride layer.

1 14. The damascene gate process of claim 11, wherein the  
2 etch stop layer is a nitride layer.

1 15. The damascene gate process of claim 11, wherein the  
2 insulating layer is a tetraethylorthosilane layer.

1           16. The damascene gate process of claim 11, wherein the  
2 protective spacer is a nitride layer.

1           17. The damascene gate process of claim 11, wherein the  
2 gate spacer is a nitride layer.

1           18. The damascene gate process of claim 11, wherein the  
2 gate conducting layer is a laminated construction with two  
3 conducting layers.

1           19. The damascene gate process of claim 18, wherein the  
2 conducting layer is a poly layer, a SiW layer, a W layer, or  
3 a silicide layer.

1           20. The damascene gate process of claim 11, before the  
2 step of forming the gate conducting layer, further comprising  
3 a step of forming a gate oxide layer on the exposed semiconductor  
4 substrate of the bottom opening.

1           21. The damascene gate process of claim 1, wherein the  
2 insulating layer is removed by HF or BHF.

1           22. The damascene gate process of claim 11, wherein the  
2 pad layer is an oxide layer.